AMENDMENTS TO THE CLAIMS

1-19. (Canceled).

20. (Currently Amended) A method for fabricating a semiconductor memory element arrangement, comprising the steps of:

forming a first electrically insulating layer on a substrate;

forming a layer system, including a floating gate and a multiple tunnel barrier arrangement formed on the floating gate, on the first electrically insulating layer;

forming a first trench structure in the layer system, the first trench structure having first trenches arranged parallel to one another and extending as far as the first electrically insulating layer;

forming a second trench structure in the layer system, the second trench structure having second trenches arranged parallel to one another and extending as far as the first electrically insulating layer, the second trenches being arranged perpendicular to the first trenches;

forming, in the first and second trench structures, a first gate electrode adjacent to the floating gate through which first gate electrode electrical charge is ~~can be~~ fed or ~~can be~~ dissipated from; and

forming, in the first and second trench structures, a second gate electrode adjacent to the multiple tunnel barrier arrangement, wherein through the second gate electrode an electrical charge transmission of the multiple tunnel barrier arrangement can be controlled.

21. (Previously Presented) The method as claimed in claim 20, wherein the steps of forming the first and second trench structures comprise the steps of:

forming a second electrically insulating layer on the multiple tunnel barrier arrangement; and

patterning the second electrically insulating layer in accordance with the first and second trench structures.

22. (Previously Presented) The method as claimed in claim 21, wherein the step of patterning the second electrically insulating layer comprises the steps of:

performing a first photolithography step by using a first photomask having a pattern of parallel strip-type openings whose width corresponds to the minimum feature size of the first trenches; and

performing a second photolithography step using a second photomask having a pattern of parallel strip-type openings which are arranged perpendicular to the strip-type openings of the first photomask and whose width corresponds to the minimum feature size of the second trenches.

23. (Previously Presented) The method as claimed in claim 22, further comprising the step of, after the first photolithography step and before the second photolithography step, forming spacers on the second electrically insulating layer in the first trenches.

24. (Previously Presented) The method as claimed in claim 20, wherein the first trenches have a smaller width than the second trenches.

25. (Previously Presented) The method as claimed in claim 20, wherein the first and second gate electrodes are formed as spacers in the second trenches of the second trench structure.

26. (Previously Presented) The method as claimed in claim 21, wherein the step of forming the first gate electrode in the first and second trench structures comprises the steps of:

applying a third electrically insulating layer on the sidewalls of the first and second trench structures; and

applying a first polysilicon layer on the third electrically insulating layer with filling of the width of the first trenches and formation of first polysilicon spacers in the second trenches in order to form the first gate electrode.

27. (Previously Presented) The method as claimed in claim 26, wherein the step of forming the second gate electrode in the first and second trench structures comprises the steps of:

applying a fourth electrically insulating layer on the first polysilicon layer; and

applying a second polysilicon layer on the third and fourth electrically insulating layers with filling of the width of the first trenches and formation of second polysilicon spacers in the second trenches in order to form the second gate electrode.

28. (Previously Presented) The method as claimed in claim 27, wherein the first, second, third and fourth electrically insulating layers are formed from silicon nitride or silicon dioxide.

29. (Previously Presented) The method as claimed in claim 20, wherein the first and second gate electrodes are formed from polysilicon.

30. (Previously Presented) The method as claimed in claim 20, wherein the multiple tunnel barrier arrangement comprises a layer stack of an alternating layer sequence of semiconducting and insulating layers.

31. (Previously Presented) The method as claimed in claim 30, wherein the semiconducting layers of the layer stack are formed from undoped polysilicon.

32. (Previously Presented) The method as claimed in claim 30, wherein the insulating layers of the layer stack are formed from silicon nitride or silicon dioxide.

33. (Previously Presented) The method as claimed in claim 30, wherein the semiconducting layers of the layer stack are formed with a thickness in a range of 30 to 50 nm and the insulating layers are formed with a thickness in a range of 2 to 4 nm.

34. (Previously Presented) The method as claimed in claim 30, wherein the semiconducting layers of the layer stack are formed with a thickness and also a grain size of at most 2 nm and the insulating layers are formed with a thickness of at most 1.5 nm.

35. (Currently Amended) A method for operating a semiconductor memory element arrangement having a first electrically insulating layer formed on a substrate and a layer system comprising a floating gate and a tunnel barrier arrangement formed on the floating gate, the layer system being formed on the first electrically insulating layer and forming a multiple tunnel barrier, wherein first and second gate electrodes are formed in a first trench structure formed in the layer system, the first trench structure including first trenches arranged parallel to one another and extending as far as the first electrically insulating layer, and a second trench structure formed in the layer system, the second trench structure including second trenches arranged parallel to one another and perpendicular to the first trenches and extending as far as the first insulating layer, the method comprising the steps of:

reading an [[the]] electrical potential on the floating gate via the first gate electrode; and

controlling an [[the]] electrical charge transmission of the tunnel barrier arrangement via the second gate electrode.

36. (Previously Presented) The method as claimed in claim 35, further comprising the step of reading data of the semiconductor memory element arrangement

by applying an electrical voltage to the first gate electrode with the second gate electrode free of voltage.

37. (Previously Presented) The method as claimed in claim 35, further comprising the step of writing or erasing data of the semiconductor memory element arrangement by applying an electrical voltage to the second gate electrode with the first gate electrode free of voltage.

38. (Withdrawn) A semiconductor memory element arrangement, in which a plurality of semiconductor memory elements are arranged in a matrix-like manner in a plurality of rows and columns, each semiconductor memory element comprising:

an electrically insulating layer formed on a substrate;

a layer system formed on the electrically insulating layer, wherein the layer system includes a floating gate and a tunnel barrier arrangement formed on the floating gate and forming a multiple tunnel barrier;

a first trench structure formed in the layer system and having first trenches arranged parallel to one another and extending as far as the electrically insulating layer;

a second trench structure formed in the layer system and having second trenches arranged parallel to one another and perpendicular to the first trenches and extending as far as the electrically insulating layer;

a first gate electrode formed in the first and second trench structures and adjacent to the floating gate, wherein the first gate electrode determines the charge carriers stored in the floating gate; and

a second gate electrode formed in the first and second trench structures and adjacent to the tunnel barrier arrangement, wherein via the second gate electrode the charge transmission of the tunnel barrier arrangement may be controlled.